

## Refine Search

### Search Results -

Term	Documents
(1 AND 29).PGPB,USPT.	5
(L29 AND L1).PGPB,USPT.	5

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L33

Refine Search

Recall Text

Clear

Interrupt

### Search History

 DATE: Wednesday, March 29, 2006   [Printable Copy](#)   [Create Case](#)

**Set**  
**Name Query**  
 side by  
 side

**Hit**  
**Count**  
**Set**  
**Name**  
 result  
 set

*DB=PGPB,USPT; PLUR=YES; OP=OR*
L33 L29 and l1
5 L33
L32 L29 and l2
4 L32
L31 L29 and l4
2 L31
L30 L29 and l3
2 L30
L29 (710/107-317, 200-244 )![CCLS]
6968 L29
*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*
L28 710/107-317, 200-244
17 L28
L27 L23 and l13
0 L27
L26 L23 and l12
2 L26
L25 L23 and l11
7 L25
L24 L23 and l6
13 L24

<u>L23</u>	l1 and (dram\$1 or dynamic\$3 near4 memor\$4)	93	<u>L23</u>
<u>L22</u>	l1 and (dram\$1 or dynamic\$3 near4 memor\$4)d	6495335	<u>L22</u>
<u>L21</u>	l4 and l13	0	<u>L21</u>
<u>L20</u>	l4 and l12	1	<u>L20</u>
<u>L19</u>	l4 and l11	5	<u>L19</u>
<u>L18</u>	l4 and l6	9	<u>L18</u>
<u>L17</u>	l2 and l13	0	<u>L17</u>
<u>L16</u>	l2 and l12	4	<u>L16</u>
<u>L15</u>	l2 and l11	-13	<u>L15</u>
<u>L14</u>	l2 and l6	23	<u>L14</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L13</u>	(716/5-18 )![CCLS]	6480	<u>L13</u>
<u>L12</u>	(712/31-40)[CCLS]	1523	<u>L12</u>
<u>L11</u>	(712/16-43)[CCLS]	3913	<u>L11</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L10</u>	l1 and host\$3	72	<u>L10</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L9</u>	L7 and (master or host\$3)	0	<u>L9</u>
<u>L8</u>	L7 and host\$3	0	<u>L8</u>
<u>L7</u>	5822606.pn. and host\$3	0	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	11961	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	L4 and multimedia	5	<u>L5</u>
<u>L4</u>	L3 and (dram\$1 or dynamic\$3 near4 memor\$4)	31	<u>L4</u>
<u>L3</u>	L2 and vector near3 register\$1	58	<u>L3</u>
<u>L2</u>	L1 and load and store	140	<u>L2</u>
<u>L1</u>	vector near15 scalar and (one or snple ) near3 (chip or chipset) and (arbitrat\$5 or switch\$5 or mux or multiplex\$5) near8 (data or media or stream\$1 or input\$1)	211	<u>L1</u>

END OF SEARCH HISTORY